

240pin Unbuffered DDR2 SDRAM MODULE

Based on 64Mx8 DDR2 SDRAM D Die

Features

• Performance:

Speed Sort		PC2-5300	PC2-6400	Unit
		-3C	-AC	
DIMM $\overline{\text{CAS}}$ Latency*		5	6	
f _{CK}	Clock Frequency	333	400	MHz
t _{CK}	Clock Cycle	3	2.5	ns
f _{DQ}	DQ Burst Frequency	667	800	MHz

- JEDEC Standard 240-pin Dual In-Line Memory Module
- 64Mx64 and 128Mx64 DDR2 Unbuffered DIMM based on 64Mx8 DDR2 SDRAM D die
- Intended for 333MHz, and 400MHz applications
- Inputs and outputs are SSTL-18 compatible
- $V_{DD} = V_{DDQ} = 1.8V \pm 0.1V$
- SDRAMs have 4 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges
- Bi-directional data strobe with one clock cycle preamble and one-half clock post-amble
- Address and control signals are fully synchronous to positive clock edge

- Programmable Operation:
 - Device $\overline{\text{CAS}}$ Latency: 3, 4, 5
 - Burst Type: Sequential or Interleave
 - Burst Length: 4, 8
 - Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 14/10/1 Addressing (row/column/rank) – 512MB
- 14/10/2 Addressing (row/column/rank) – 1GB
- 7.8 μs Max. Average Periodic Refresh Interval
- Serial Presence Detect
- Gold contacts
- SDRAMs in 60 ball BGA Package
- RoHS compliance

Description

M2Y51H64TU88D0B, M2Y1GH64TU8HD0B, M2Y51H64TU88D6B and M2Y1GH64TU8HD6B are 240-Pin Double Data Rate 2 (DDR2) Synchronous DRAM Unbuffered Dual In-Line Memory Module (UDIMM), organized as one-rank 64Mx64 and two ranks 128Mx64 high-speed memory array. M2Y51H64TU88D0B and M2Y51H64TU88D6B use eight 64Mx8 DDR2 SDRAMs. M2Y1GH64TU8HD0B and M2Y1GH64TU8HD6B use sixteen 64Mx8 DDR2 SDRAMs. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All Elixir DDR2 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint.

The DIMM is intended for use in applications operating up to 333MHz and 400MHz clock speeds and achieves high-speed data transfer rates of up to 667MHz and 800MHz. Prior to any access operation, the device $\overline{\text{CAS}}$ latency and burst / length / operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0 and BA1 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial 2,048-bit EEPROM using a standard IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

Ordering Information

Part Number	Speed			Organization	Leads	Power	Note
M2Y51H64TU88D0B-3C	333MHz (3.00ns@ CL = 5)	DDR2-667	PC2-5300	64Mx64	Green	1.8 V	
M2Y51H64TU88D0B-AC	400MHz (2.50ns@ CL = 5)	DDR2-800	PC2-6400				
M2Y51H64TU88D6B-3C	333MHz (3.00ns@ CL = 5)	DDR2-667	PC2-5300				
M2Y51H64TU88D6B-AC	400MHz (2.50ns@ CL = 5)	DDR2-800	PC2-6400				
M2Y1GH64TU8HD0B-3C	333MHz (3.00ns@ CL = 5)	DDR2-667	PC2-5300	128Mx64			
M2Y1GH64TU8HD0B-AC	400MHz (2.50ns@ CL = 5)	DDR2-800	PC2-6400				
M2Y1GH64TU8HD6B-3C	333MHz (3.00ns@ CL = 5)	DDR2-667	PC2-5300				
M2Y1GH64TU8HD6B-AC	400MHz (2.50ns@ CL = 5)	DDR2-800	PC2-6400				

Pin Description

CK0-CK2, $\overline{\text{CK0}}\text{-}\overline{\text{CK2}}$	Differential Clock Inputs	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	DQS0-DQS8	Bidirectional data strobes
$\overline{\text{RAS}}$	Row Address Strobe	DM0-DM8	Input Data Mask/High Data Strokes
$\overline{\text{CAS}}$	Column Address Strobe	$\overline{\text{DQS0}}\text{-}\overline{\text{DQS8}}$	Differential data strobes
$\overline{\text{WE}}$	Write Enable	V_{DD}	Power (1.8V)
$\overline{\text{CS0}}, \overline{\text{CS1}}$	Chip Selects	V_{REF}	Ref. Voltage for SSTL_18 inputs
A0-A9, A11-A13	Address Inputs	V_{DDSPD}	Serial EEPROM positive power supply
A10/AP	Column Address Input/Auto-precharge	V_{SS}	Ground
BA0, BA1	SDRAM Bank Address Inputs	SCL	Serial Presence Detect Clock Input
$\overline{\text{RESET}}$	Reset pin	SDA	Serial Presence Detect Data input/output
ODT0, ODT1	Active termination control lines	SA0-2	Serial Presence Detect Address Inputs
NC	No Connect		

Note: ODT1, CKE1 and $\overline{\text{CS1}}$ are only support in 1GB module type.

Pinout

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V _{REF}	42	NC	82	V _{SS}	121	V _{SS}	162	NC	202	DM4
2	V _{SS}	43	NC	83	DQS4	122	DQ4	163	V _{SS}	203	NC
3	DQ0	44	V _{SS}	84	DQS4	123	DQ5	164	NC	204	V _{SS}
4	DQ1	45	NC	85	V _{SS}	124	V _{SS}	165	NC	205	DQ38
5	V _{SS}	46	NC	86	DQ34	125	DM0	166	V _{SS}	206	DQ39
6	DQS0	47	V _{SS}	87	DQ35	126	NC	167	NC	207	V _{SS}
7	DQS0	48	NC	88	V _{SS}	127	V _{SS}	168	NC	208	DQ44
8	V _{SS}	49	NC	89	DQ40	128	DQ6	169	V _{SS}	209	DQ45
9	DQ2	50	V _{SS}	90	DQ41	129	DQ7	170	V _{DDQ}	210	V _{SS}
10	DQ3	51	V _{DDQ}	91	V _{SS}	130	V _{SS}	171	CKE1/NC	211	DM5
11	V _{SS}	52	CKE0	92	DQS5	131	DQ12	172	V _{DD}	212	NC
12	DQ8	53	V _{DD}	93	DQS5	132	DQ13	173	NC	213	V _{SS}
13	DQ9	54	NC	94	V _{SS}	133	V _{SS}	174	NC	214	DQ46
14	V _{SS}	55	NC	95	DQ42	134	DM1	175	V _{DDQ}	215	DQ47
15	DQS1	56	V _{DDQ}	96	DQ43	135	NC	176	A12	216	V _{SS}
16	DQS1	57	A11	97	V _{SS}	136	V _{SS}	177	A9	217	DQ52
17	V _{SS}	58	A7	98	DQ48	137	CK1	178	V _{DD}	218	DQ53
18	NC	59	V _{DD}	99	DQ49	138	CK1	179	A8	219	V _{SS}
19	NC	60	A5	100	V _{SS}	139	V _{SS}	180	A6	220	CK2
20	V _{SS}	61	A4	101	SA2	140	DQ14	181	V _{DDQ}	221	CK2
21	DQ10	62	V _{DDQ}	102	NC	141	DQ15	182	A3	222	V _{SS}
22	DQ11	63	A2	103	V _{SS}	142	V _{SS}	183	A1	223	DM6
23	V _{SS}	64	V _{DD}	104	DQS6	143	DQ20	184	V _{DD}	224	NC
24	DQ16	KEY		105	DQS6	144	DQ21	KEY		225	V _{SS}
25	DQ17	65	V _{SS}	106	V _{SS}	145	V _{SS}	185	CK0	226	DQ54
26	V _{SS}	66	V _{SS}	107	DQ50	146	DM2	186	CK0	227	DQ55
27	DQS2	67	V _{DD}	108	DQ51	147	NC	187	V _{DD}	228	V _{SS}
28	DQS2	68	NC	109	V _{SS}	148	V _{SS}	188	A0	229	DQ60
29	V _{SS}	69	V _{DD}	110	DQ56	149	DQ22	189	V _{DD}	230	DQ61
30	DQ18	70	A10/AP	111	DQ57	150	DQ23	190	BA1	231	V _{SS}
31	DQ19	71	BA0	112	V _{SS}	151	V _{SS}	191	V _{DDQ}	232	DM7
32	V _{SS}	72	V _{DDQ}	113	DQS7	152	DQ28	192	RAS	233	NC
33	DQ24	73	WE	114	DQS7	153	DQ29	193	CS0	234	V _{SS}
34	DQ25	74	CAS	115	V _{SS}	154	V _{SS}	194	V _{DDQ}	235	DQ62
35	V _{SS}	75	V _{DDQ}	116	DQ58	155	DM3	195	ODT0	236	DQ63
36	DQS3	76	CS1/NC	117	DQ59	156	NC	196	A13	237	V _{SS}
37	DQS3	77	ODT1/NC	118	V _{SS}	157	V _{SS}	197	V _{DD}	238	V _{DDSPD}
38	V _{SS}	78	V _{DDQ}	119	SDA	158	DQ30	198	V _{SS}	239	SA0
39	DQ26	79	V _{SS}	120	SCL	159	DQ31	199	DQ36	240	SA1
40	DQ27	80	DQ32			160	V _{SS}	200	DQ37		
41	V _{SS}	81	DQ33			161	NC	201	V _{SS}		

Note:

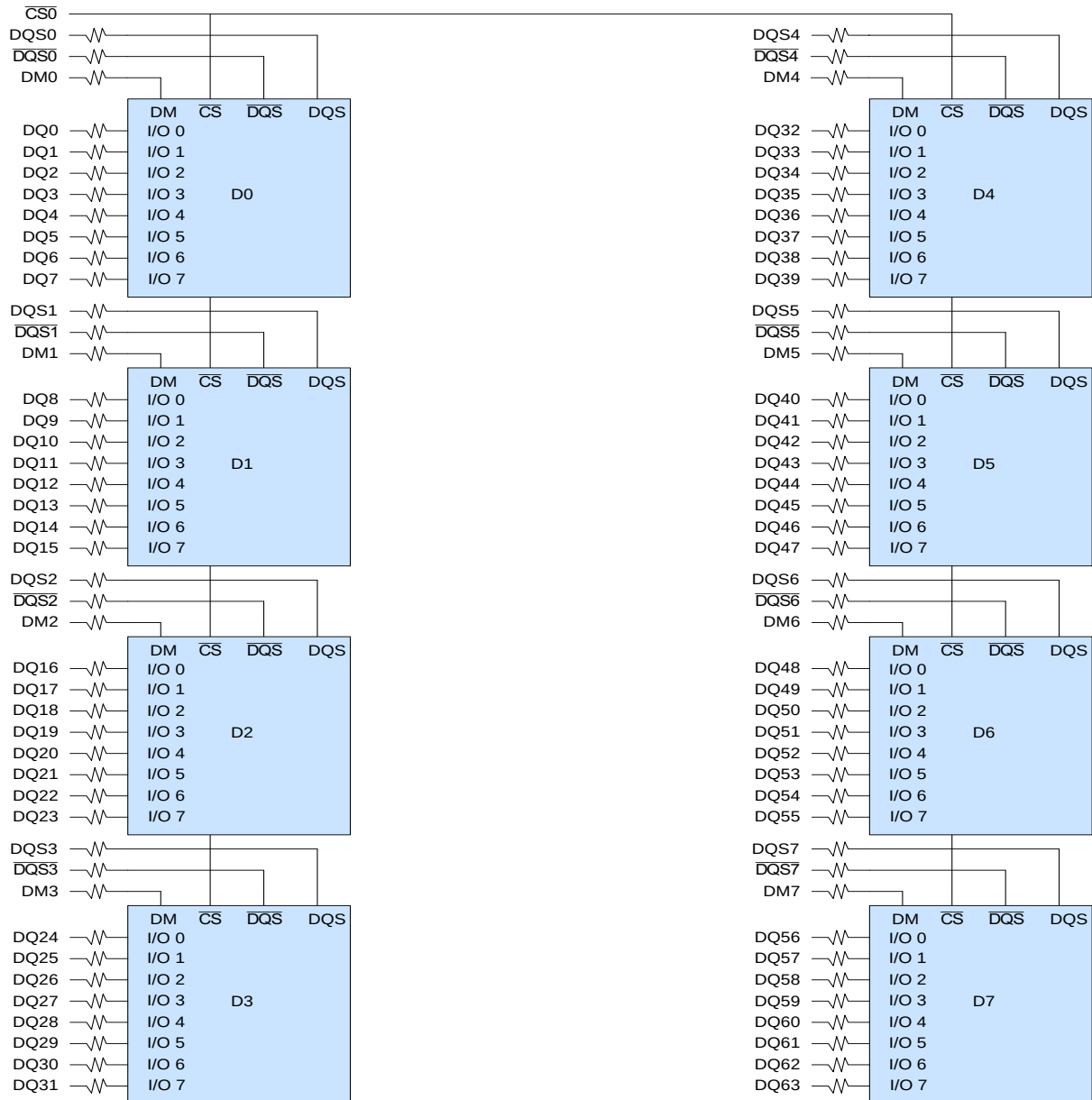
1. NC = No Connect.
2. CS1, ODT1 and CKE1 (Pins 76, 77 and 171) are only support in 1GB module type.

Input/Output Functional Description

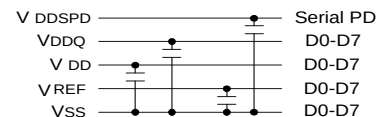
Symbol	Type	Polarity	Function
CK0, CK1, CK2	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. All the DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks.
$\overline{\text{CK0}}, \overline{\text{CK1}}, \overline{\text{CK2}}$	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{\text{CS0}}, \overline{\text{CS1}}$	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{\text{RAS}}, \overline{\text{CAS}}, \overline{\text{WE}}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{\text{RAS}}, \overline{\text{CAS}}, \overline{\text{WE}}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL-18 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
ODT0, ODT1	Input	Active High	On-Die Termination control signals
BA0, BA1	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 – A9 A10/AP A11 – A13	(SSTL)	-	During a Bank Activate command cycle, A0-A14 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 – DQ63	(SSTL)	Active High	Data and Check Bit Input/Output pins.
$V_{\text{DD}}, V_{\text{SS}}$	Supply		Power and ground for the DDR2 SDRAM input buffers and core logic
$\text{DQS0} - \text{DQS8}$ $\overline{\text{DQS0}} - \overline{\text{DQS8}}$	(SSTL)	Negative and Positive Edge	Data strobe for input and output data
DM0 – DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
SA0 – SA2		-	Address inputs. Connected to either V_{DD} or V_{SS} on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pull-up.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pull-up.
V_{DDSPD}	Supply		Serial EEPROM positive power supply.

Functional Block Diagram

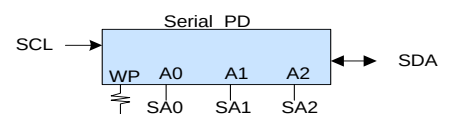
(512MB, 1 Rank, 64Mx8 DDR2 SDRAMs)



BA0-BA1 ——— BA0-BA2: SDRAMs D0-D7
 A0-A13 ——— A0-A13: SDRAMs D0-D7
 RAS ——— RAS: SDRAMs D0-D7
 CAS ——— CAS: SDRAMs D0-D7
 WE ——— WE: SDRAMs D0-D7
 CKE0 ——— CKE: SDRAMs D0-D7
 ODT0 ——— ODT: SDRAMs D0-D7

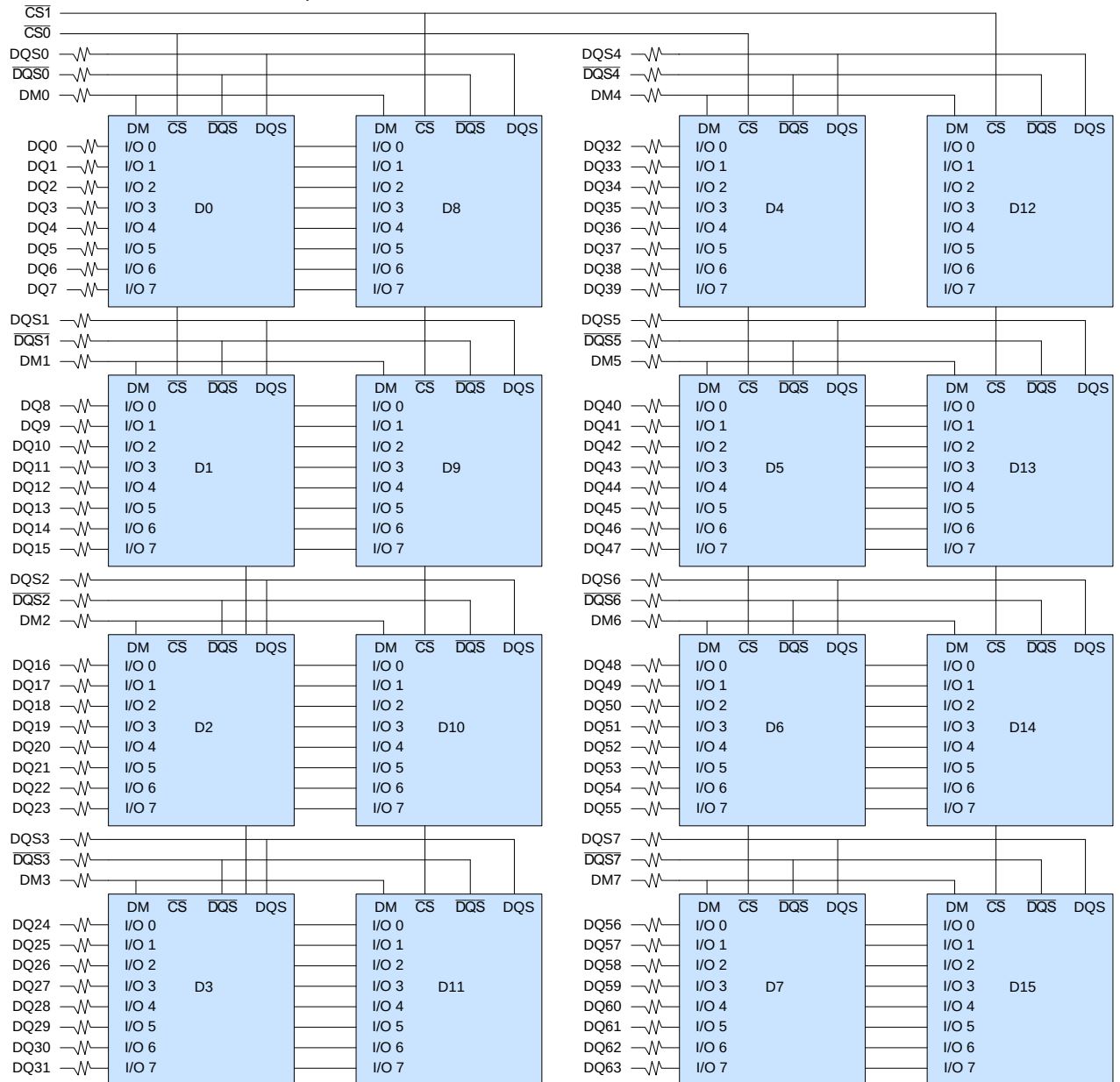


- Notes :
1. DQ-to-I/O wiring may be changed within a byte.
 2. DQ/DQS/DM/CKE/CS relationships are maintained as shown.
 3. DQ/DQS/DQS resistors are 22 Ohms +/- 5%
 4. BAX, Ax, RAS, CAS, WE resistors are 5.1 Ohms +/- 5%
 5. Address and control resistors are 22 Ohms +/- 5%



Functional Block Diagram

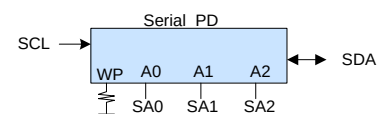
(1GB, 2 Rank, 64Mx8 DDR2 SDRAMs)



BA0-BA1 : SDRAMs D0-D15
 A0-A13 : SDRAMs D0-D15
 RAS : SDRAMs D0-D15
 CAS : SDRAMs D0-D15
 WE : SDRAMs D0-D15
 CKE0 : SDRAMs D0-D7
 CKE1 : SDRAMs D8-D15
 ODT0 : SDRAMs D0-D7
 ODT1 : SDRAMs D8-D15

V DDSPD : Serial PD
 V DDQ : D0-D15
 V DD : D0-D15
 VREF : D0-D15
 VSS : D0-D15

- Notes :
1. DQ-to-I/O wiring may be changed within a byte.
 2. DQ/DQS/DM/CKE/CS relationships are maintained as shown.
 3. DQ/DQS/DQS resistors are 22 Ohms +/- 5%
 4. BAX, Ax, RAS, CAS, WE resistors are 5.1 Ohms +/- 5%
 5. Address and control resistors are 22 Ohms +/- 5%



Serial Presence Detect – Part 1 of 2 (512MB)

64Mx64 1 RANK UNBUFFERED DDR2 SDRAM DIMM based on 64Mx8,1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		-3C	-AC	-3C	-AC	
0	Number of Serial PD Bytes Written during Production	128		80		
1	Total Number of Bytes in Serial PD device	256		08		
2	Fundamental Memory Type	DDR2 SDRAM		08		
3	Number of Row Addresses on Assembly	14		0E		
4	Number of Column Addresses on Assembly	10		0A		
5	Number of DIMM Ranks	1 rank, Height=30mm		60		
6	Data Width of Assembly	X64		40		
7	Reserved	Undefined		00		
8	Voltage Interface Level of this Assembly	SSTL_1.8V		05		
9	DDR2 SDRAM Device Cycle Time at CL=X	3	2.5	30	25	
10	DDR2 SDRAM Device Access Time from Clock at CL=X	0.45	0.40	45	40	
11	DIMM Configuration Type	Non parity/ECC		00		
12	Refresh Rate/Type	7.8μs/self		82		
13	Primary DDR2 SDRAM Width	X8		08		
14	Error Checking DDR2 SDRAM Device Width	Undefined		00		
15	Reserved	Undefined		00		
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8		0C		
17	DDR2 SDRAM Device Attributes: Number of Device Banks	4		04		
18	DDR2 SDRAM Device Attributes: CAS Latencies Supported	3,4,5		38		
19	DIMM Mechanical Characteristics	<4.1(mm)		01		
20	DDR2 SDRAM DIMM Type Information	Regular UDIMM (133.35mm)		02		
21	DDR2 SDRAM Module Attributes:	Normal DIMM		00		
22	DDR2 SDRAM Device Attributes: General	Support weak Driver, 50Ω ODT, and PASR		07		
23	Minimum Clock Cycle at CL=X-1	3.75ns		3D		
24	Maximum Data Access Time from Clock at CL=X-1	0.5ns		50		
25	Minimum Clock Cycle Time at CL=X-2	5.0ns		50		
26	Maximum Data Access Time from Clock at CL=X-2	0.6ns		60		
27	Minimum Row Precharge Time (t _{RP})	15ns	12.5ns	3C	32	
28	Minimum Row Active to Row Active delay (t _{RRD})	7.5ns		1E		
29	Minimum RAS to CAS delay (t _{RCD})	15ns	12.5ns	3C	32	
30	Minimum RAS Pulse Width (t _{RAS})	45ns		2D		
31	Module Bank Density	512MB		80		
32	Address and Command Setup Time Before Clock (t _{IS})	0.2ns	0.17ns	20	17	
33	Address and Command Hold Time After Clock (t _{IH})	0.27ns	0.25ns	27	25	
34	Data Input Setup Time Before Clock (t _{DS})	0.10ns	0.05ns	10	05	
35	Data Input Hold Time After Clock (t _{DH})	0.17ns	0.12ns	17	12	
36	Write Recovery Time (t _{WR})	15ns		3C		
37	Internal Write to Read Command delay (t _{WTR})	7.5ns		1E		
38	Internal Read to Precharge delay (t _{RTP})	7.5ns		1E		
39	Reserved	Undefined		00		

Serial Presence Detect -- Part 2 of 2 (512MB)

64Mx64 1RANK UNBUFFERED DDR2 SDRAM DIMM based on 64Mx8, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		-3C	-AC	-3C	-AC	
40	Extension of Byte 41 t_{RC} and Byte 42 t_{RFC}	00: The number below a decimal point of t_{RC} and t_{RFC} are 0, t_{RFC} is less than 256ns. 30: The number below a decimal point of t_{RC} is 5, t_{RFC} is less than 256ns		06	36	
41	Minimum Core Cycle Time (t_{RC})	60.ns	57.7ns	3C	39	
42	Min. Auto Refresh Command Cycle Time (t_{RFC})	127.5ns		7F		
43	Maximum Clock Cycle Time (t_{CK})	8.0ns		80		
44	Max. DQS-DQ Skew Factor (t_{DQS})	0.24ns	0.2	18	14	
45	Read Data Hold Skew Factor (t_{QHS})	0.34ns	0.30	22	1E	
46	PLL Relock Time	Undefined		00		
47	Tcasemax, DT4R4W Delta	Undefined		00		
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi T-A DRAM)	Undefined		00		
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	Undefined		00		
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	Undefined		00		
51	DRAM Case Temperature Rise from Ambient due to precharge Power-Down (DT2P)	Undefined		00		
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	Undefined		00		
53	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3P fast)	Undefined		00		
54	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3P slow)	Undefined		00		
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	Undefined		00		
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B)	Undefined		00		
57	DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7)	Undefined		00		
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	Undefined		00		
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	Undefined		00		
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	Undefined		00		
61	Register Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit)	Undefined		00		
62	SPD Revision	1.3		13		
63	Checksum for Byte 0-62	Checksum data		92	78	
64-71	Manufacture's JEDEC ID Code	NANYA		7F7F7F0B00000000		
72-255	Reserved	Undefined		--		

Serial Presence Detect – Part 1 of 2 (1GB)

128Mx64 2 RANKs UNBUFFERED DDR2 SDRAM DIMM based on 64Mx8, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		-3C	-AC	-3C	-AC	
0	Number of Serial PD Bytes Written during Production	128		80		
1	Total Number of Bytes in Serial PD device	256		08		
2	Fundamental Memory Type	DDR2 SDRAM		08		
3	Number of Row Addresses on Assembly	14		0E		
4	Number of Column Addresses on Assembly	10		0A		
5	Number of DIMM Ranks	2 ranks, Height=30mm		61		
6	Data Width of Assembly	X64		40		
7	Reserved	Undefined		00		
8	Voltage Interface Level of this Assembly	SSTL_1.8V		05		
9	DDR2 SDRAM Device Cycle Time at CL=X	3	2.5	30	25	
10	DDR2 SDRAM Device Access Time from Clock at CL=X	0.45	0.40	45	40	
11	DIMM Configuration Type	Non parity/ECC		00		
12	Refresh Rate/Type	7.8µs/self		82		
13	Primary DDR2 SDRAM Width	X8		08		
14	Error Checking DDR2 SDRAM Device Width	Undefined		00		
15	Reserved	Undefined		00		
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8		0C		
17	DDR2 SDRAM Device Attributes: Number of Device Banks	4		04		
18	DDR2 SDRAM Device Attributes: CAS Latencies Supported	3,4,5		38		
19	DIMM Mechanical Characteristics	<4.1(mm)		01		
20	DDR2 SDRAM DIMM Type Information	Regular UDIMM (133.35mm)		02		
21	DDR2 SDRAM Module Attributes:	Normal DIMM		00		
22	DDR2 SDRAM Device Attributes: General	Support weak Driver, 50Ω ODT, and PASR		07		
23	Minimum Clock Cycle at CL=X-1	3.75ns		3D		
24	Maximum Data Access Time from Clock at CL=X-1	0.5ns		50		
25	Minimum Clock Cycle Time at CL=X-2	5.0ns		50		
26	Maximum Data Access Time from Clock at CL=X-2	0.6ns		60		
27	Minimum Row Precharge Time (t _{RP})	15ns	12.5ns	3C	32	
28	Minimum Row Active to Row Active delay (t _{RRD})	7.5ns		1E		
29	Minimum RAS to CAS delay (t _{RCD})	15ns	12.5ns	3C	32	
30	Minimum RAS Pulse Width (t _{RAS})	45ns		2D		
31	Module Bank Density	512MB		80		
32	Address and Command Setup Time Before Clock (t _{IS})	0.2ns	0.17ns	20	17	
33	Address and Command Hold Time After Clock (t _{IH})	0.27ns	0.25ns	27	25	
34	Data Input Setup Time Before Clock (t _{DS})	0.10ns	0.05ns	10	05	
35	Data Input Hold Time After Clock (t _{DH})	0.17ns	0.12ns	17	12	
36	Write Recovery Time (t _{WR})	15ns		3C		
37	Internal Write to Read Command delay (t _{WTR})	7.5ns		1E		
38	Internal Read to Precharge delay (t _{RTP})	7.5ns		1E		
39	Reserved	Undefined		00		

Serial Presence Detect – Part 2 of 2 (1GB)

128Mx64 2 RANKs UNBUFFERED DDR2 SDRAM DIMM based on 64Mx8, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		-3C	-AC	-3C	-AC	
40	Extension of Byte 41 t_{RC} and Byte 42 t_{RFC}	00: The number below a decimal point of t_{RC} and t_{RFC} are 0, t_{RFC} is less than 256ns. 30: The number below a decimal point of t_{RC} is 5, t_{RFC} is less than 256ns		06	36	
41	Minimum Core Cycle Time (t_{RC})	60.ns	57.7ns	3C	39	
42	Min. Auto Refresh Command Cycle Time (t_{RFC})	127.5ns		7F		
43	Maximum Clock Cycle Time (t_{CK})	8.0ns		80		
44	Max. DQS-DQ Skew Factor (t_{DQS})	0.24ns	0.2	18	14	
45	Read Data Hold Skew Factor (t_{QHS})	0.34ns	0.30	22	1E	
46	PLL Relock Time	Undefined		00		
47	Tcasemax, DT4R4W Delta	Undefined		00		
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi T-A DRAM)	Undefined		00		
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	Undefined		00		
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	Undefined		00		
51	DRAM Case Temperature Rise from Ambient due to precharge Power-Down (DT2P)	Undefined		00		
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	Undefined		00		
53	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3P fast)	Undefined		00		
54	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3P slow)	Undefined		00		
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	Undefined		00		
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B)	Undefined		00		
57	DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7)	Undefined		00		
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	Undefined		00		
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	Undefined		00		
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	Undefined		00		
61	Resister Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit)	Undefined		00		
62	SPD Revision	1.3		13		
63	Checksum for Byte 0-62	Checksum data		93	79	
64-71	Manufacture's JEDEC ID Code	NANYA		7F7F7F0B00000000		
72-255	Reserved	Undefined		--		

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.5 to 2.3	V
V_{DD}	Voltage on VDD supply relative to Vss	-1.0 to +2.3	V
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-0.5 to +2.3	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC operating Conditions

Symbol	Parameter	Rating	Units	Note
T_{CASE}	Operating Temperature (Ambient)	0 to 95	°C	1,2,3
T_{STG}	Storage Temperature (Plastic)	-55 to 100	°C	
I_L	Short Circuit Output Current	-5 to 5	μA	

Note:

- Case temperature is measured at top and center side of any DRAMs.
- $t_{CASE} > 85^{\circ}\text{C} \rightarrow t_{REFI} = 3.9 \mu\text{s}$
- All DRAM specification only support $0^{\circ}\text{C} < t_{CASE} < 85^{\circ}\text{C}$

DC Electrical Characteristics and Operating Conditions

($T_{CASE} = 0^{\circ}\text{C} \sim 85^{\circ}\text{C}$; $V_{DDQ} = 1.8\text{V} \pm 0.1\text{V}$; $V_{DD} = 1.8\text{V} \pm 0.1\text{V}$, See AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	1.7	1.9	V	1
V_{DDQ}	I/O Supply Voltage	1.7	1.9	V	1
V_{SS}, V_{SSQ}	Supply Voltage, I/O Supply Voltage	0	0	V	
V_{REF}	I/O Reference Voltage	$0.49V_{DDQ}$	$0.51V_{DDQ}$	V	1, 2
$V_{IH}(\text{DC})$	Input High (Logic1) Voltage	$V_{REF} + 0.125$	$V_{DDQ} + 0.3$	V	1
$V_{IL}(\text{DC})$	Input Low (Logic0) Voltage	-0.3	$V_{REF} - 0.125$	V	1

Note:

- Inputs are not recognized as valid until V_{REF} stabilizes.
- V_{REF} is expected to be equal to $0.5 V_{DDQ}$ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.

Environmental Parameters

Symbol	Parameter	Rating	Units	Note
T_{OPR}	Module Operating Temperature Range (ambient)	0 to 55	°C	3
H_{OPR}	Operating Humidity (relative)	10 to 90	%	
T_{STG}	Storage Temperature (Plastic)	-55 to 100	°C	1
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

Note:

- Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Up to 9850 ft.
- The component maximum case temperature shall not exceed the value specified in the component spec.

Operating, Standby, and Refresh Currents

$T_{CASE} = 0^{\circ}C \sim 85^{\circ}C$; $V_{DDQ} = V_{DD} = 1.8V \pm 0.1V$ (512MB, 1 Rank, 64Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-5300	PC2-6400	Unit
I_{DD0}	Operating Current: one bank; active/precharge; $t_{RC} = t_{RC} (MIN)$; $t_{CK} = t_{CK} (MIN)$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	TBD	TBD	mA
I_{DD1}	Operating Current: one bank; active/read/precharge; Burst = 2; $t_{RC} = t_{RC} (MIN)$; $CL=2.5$; $t_{CK} = t_{CK} (MIN)$; $I_{OUT} = 0mA$; address and control inputs changing once per clock cycle	TBD	TBD	mA
I_{DD2P}	Precharge Power-Down Standby Current: all banks idle; power-down mode; $CKE \leq V_{IL} (MAX)$; $t_{CK} = t_{CK} (MIN)$	TBD	TBD	mA
I_{DD2N}	Idle Standby Current: $CS \geq V_{IH} (MIN)$; all banks idle; $CKE \geq V_{IH} (MIN)$; $t_{CK} = t_{CK} (MIN)$; address and control inputs changing once per clock cycle	TBD	TBD	mA
I_{DD2Q}	Precharge Quiet Standby Current: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK} (MIN)$; Other control and address inputs are stable, Data bus inputs are floating.	TBD	TBD	mA
I_{DD3PF}	Active Power-Down Current: All banks open; $t_{CK} = t_{CK} (MIN)$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to low (Fast Power-down Exit).	TBD	TBD	mA
I_{DD3PS}	Active Power-Down Current: All banks open; $t_{CK} = t_{CK} (MIN)$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to high (Slow Power-down Exit).	TBD	TBD	mA
I_{DD3N}	Active Standby Current: one bank; active/precharge; $CS \geq V_{IH} (MIN)$; $CKE \geq V_{IH} (MIN)$; $t_{RC} = t_{RAS} (MAX)$; $t_{CK} = t_{CK} (MIN)$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	TBD	TBD	mA
I_{DD4W}	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; $CL=2.5$; $t_{CK} = t_{CK} (MIN)$	TBD	TBD	mA
I_{DD4R}	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; $CL = 2.5$; $t_{CK} = t_{CK} (MIN)$; $I_{OUT} = 0mA$	TBD	TBD	mA
I_{DD5}	Auto-Refresh Current: $t_{RC} = t_{RFC} (MIN)$	TBD	TBD	mA
I_{DD6}	Self-Refresh Current: $CKE \leq 0.2V$	TBD	TBD	mA
I_{DD7}	Operating Current: four bank; four bank interleaving with $BL = 4$, address and control inputs randomly changing; 50% of data changing at every transfer; $t_{RC} = t_{RC} (min)$; $I_{OUT} = 0mA$.	TBD	TBD	mA

Operating, Standby, and Refresh Currents

$T_{CASE} = 0^{\circ}C \sim 85^{\circ}C$; $V_{DDQ} = V_{DD} = 1.8V \pm 0.1V$ (1GB, 2 Banks, 64Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-5300	PC2-6400	Unit
I_{DD0}	Operating Current: one bank; active/precharge; $t_{RC} = t_{RC} (MIN)$; $t_{CK} = t_{CK} (MIN)$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	TBD	TBD	mA
I_{DD1}	Operating Current: one bank; active/read/precharge; Burst = 2; $t_{RC} = t_{RC} (MIN)$; $CL=2.5$; $t_{CK} = t_{CK} (MIN)$; $I_{OUT} = 0mA$; address and control inputs changing once per clock cycle	TBD	TBD	mA
I_{DD2P}	Precharge Power-Down Standby Current: all banks idle; power-down mode; $CKE \leq V_{IL} (MAX)$; $t_{CK} = t_{CK} (MIN)$	TBD	TBD	mA
I_{DD2N}	Idle Standby Current: $CS \geq V_{IH} (MIN)$; all banks idle; $CKE \geq V_{IH} (MIN)$; $t_{CK} = t_{CK} (MIN)$; address and control inputs changing once per clock cycle	TBD	TBD	mA
I_{DD2Q}	Precharge Quiet Standby Current: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK} (MIN)$; Other control and address inputs are stable, Data bus inputs are floating.	TBD	TBD	mA
I_{DD3PF}	Active Power-Down Current: All banks open; $t_{CK} = t_{CK} (MIN)$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to low (Fast Power-down Exit).	TBD	TBD	mA
I_{DD3PS}	Active Power-Down Current: All banks open; $t_{CK} = t_{CK} (MIN)$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to high (Slow Power-down Exit).	TBD	TBD	mA
I_{DD3N}	Active Standby Current: one bank; active/precharge; $CS \geq V_{IH} (MIN)$; $CKE \geq V_{IH} (MIN)$; $t_{RC} = t_{RAS} (MAX)$; $t_{CK} = t_{CK} (MIN)$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	TBD	TBD	mA
I_{DD4W}	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; $CL=2.5$; $t_{CK} = t_{CK} (MIN)$	TBD	TBD	mA
I_{DD4R}	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; $CL = 2.5$; $t_{CK} = t_{CK} (MIN)$; $I_{OUT} = 0mA$	TBD	TBD	mA
I_{DD5}	Auto-Refresh Current: $t_{RC} = t_{RFC} (MIN)$	TBD	TBD	mA
I_{DD6}	Self-Refresh Current: $CKE \leq 0.2V$	TBD	TBD	mA
I_{DD7}	Operating Current: four bank; four bank interleaving with $BL = 4$, address and control inputs randomly changing; 50% of data changing at every transfer; $t_{RC} = t_{RC} (min)$; $I_{OUT} = 0mA$.	TBD	TBD	mA

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter	PC2-5300		PC2-6400		Unit
		Min.	Max.	Min.	Max.	
t _{AC}	DQ output access time from CK/ $\overline{\text{CK}}$	-0.45	+0.45	-0.40	+0.40	ns
td _{Q_{CK}}	DQS output access time from CK/ $\overline{\text{CK}}$	-0.40	+0.40	-0.35	+0.35	ns
t _{CH}	CK high-level width	0.45	0.55	0.45	0.55	tCK
t _{CL}	CK low-level width	0.45	0.55	0.45	0.55	tCK
t _{HP}	Minimum half clk period for any given cycle; defined by clk high (t _{CH}) or clk low (t _{CL}) time	t _{CH} or t _{CL}	-	t _{CH} or t _{CL}	-	tCK
t _{CK}	Clock Cycle Time	3	8	2.5	8	ns
t _{DS}	DQ and DM input setup time(differential data strobe)	0.1	-	0.05	-	ns
t _{DH}	DQ and DM input hold time(differential data strobe)	0.175	-	0.125	-	ns
t _{IPW}	Input pulse width	0.6	-	0.6	-	tCK
td _{IPW}	DQ and DM input pulse width (each input)	0.35	-	0.35	-	tCK
t _{HZ}	Data-out high-impedance time from CK/ $\overline{\text{CK}}$	-	t _{ACmax}	-	t _{ACmax}	ns
t _{LZ(DQS)}	DQS low-impedance time from CK/ $\overline{\text{CK}}$	t _{ACmin}	t _{ACmax}	t _{ACmin}	t _{ACmax}	ns
t _{LZ(DQ)}	DQ low-impedance time from CK/ $\overline{\text{CK}}$	2t _{AC min}	t _{AC max}	2t _{AC min}	t _{AC max}	ns
td _{QSQ}	DQS-DQ skew (DQS & associated DQ signals)	-	0.24	-	0.20	ns
t _{QHS}	Data hold Skew Factor	-	0.34	-	0.3	ns
t _{QH}	Data output hold time from DQS	t _{HP} - t _{QHS}	-	t _{HP} - t _{QHS}	-	ns
td _{QSS}	Write command to 1st DQS latching transition	-0.25	+0.25	-0.25	+0.25	tCK
td _{QSL(H)}	DQS input low (high) pulse width (write cycle)	0.35	-	0.35	-	tCK
t _{DSS}	DQS falling edge to CK setup time (write cycle)	0.2	-	0.2	-	tCK
t _{DSH}	DQS falling edge hold time from CK (write cycle)	0.2	-	0.2	-	tCK
t _{MRD}	Mode register set command cycle time	2	-	2	-	tCK
t _{WPST}	Write postamble	0.40	0.60	0.40	0.60	tCK
t _{WPRE}	Write preamble	0.35	-	0.35	-	tCK
t _{IH}	Address and control input hold time	275	-	250	-	ps
t _{IS}	Address and control input setup time	200	-	175	-	ps
t _{RPRE}	Read preamble	0.90	1.10	0.90	1.10	tCK
t _{RPST}	Read postamble	0.40	0.60	0.40	0.60	tCK
t _{RRD}	Active bank A to Active bank B command	7.5	-	7.5	-	ns
t _{Delay}	Minimum time clocks remains ON after CKE asynchronously drops Low	t _{IS} + t _{CK} + t _{IH}	-	t _{IS} + t _{CK} + t _{IH}	-	ns
t _{REFI}	Average Periodic Refresh Interval (85°C < T _{CASE} ≤ 95°C)	3.9		3.9		μs
	Average Periodic Refresh Interval (0°C ≤ T _{CASE} ≤ 85°C)	7.8		7.8		μs
to _{IT}	OCD drive mode output delay	0	12	0	12	ns
t _{CCD}	$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$	2		2		tCK

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 2 of 2)

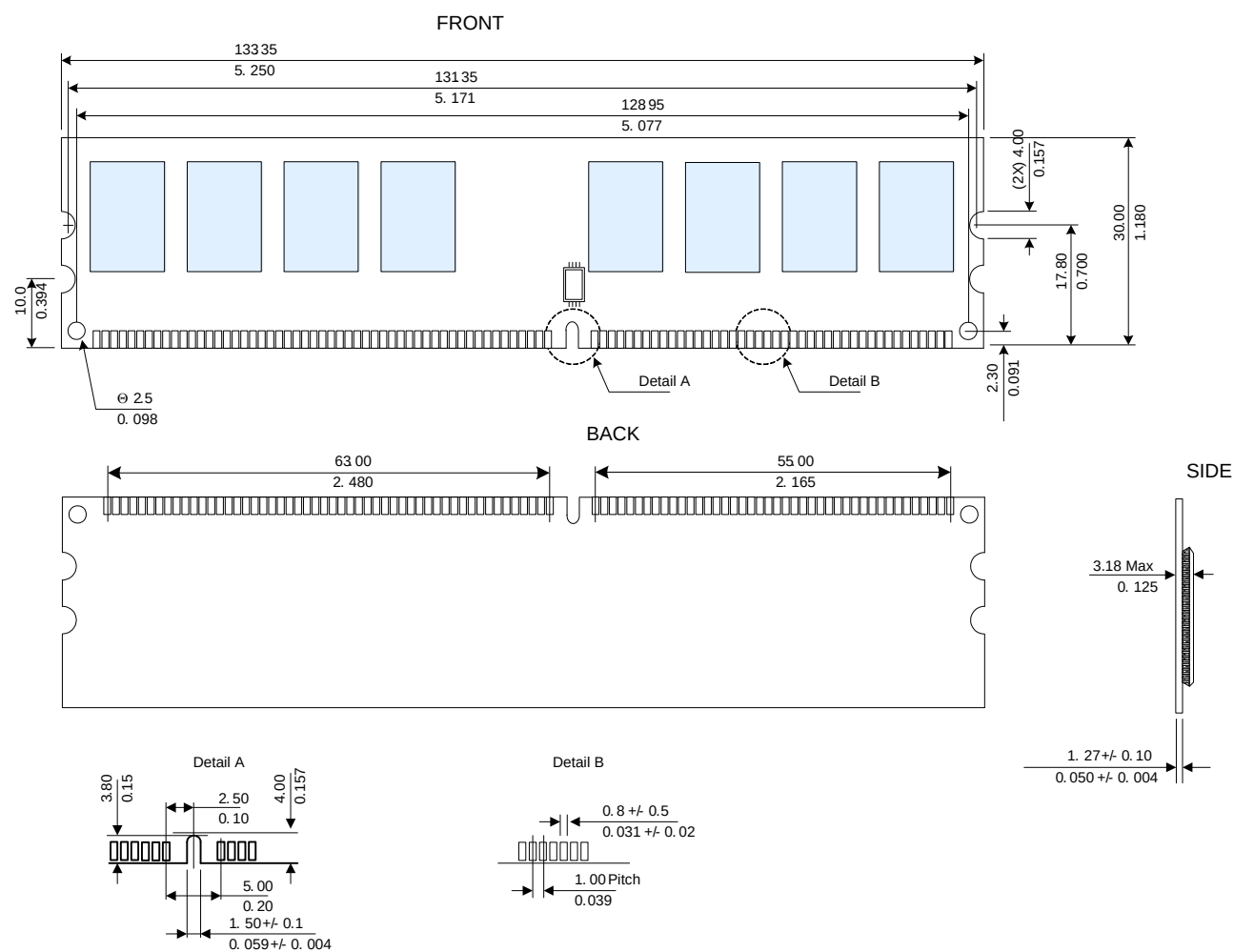
Symbol	Parameter	PC2-5300		PC2-6400		Unit
		Min.	Max.	Min.	Max.	
t _{WR}	Write recovery time without Auto-Precharge	15	-	15	-	ns
WR	Write recovery time with Auto-Precharge	t _{WR} /t _{CK}	-	t _{WR} /t _{CK}	-	t _{CK}
t _{DAL}	Auto precharge write recovery + precharge time	WR+t _{RP}	-	WR+t _{RP}	-	t _{CK}
t _{WTR}	Internal write to read command delay	7.5	-	7.5	-	ns
t _{RTP}	Internal read to precharge command delay	7.5	-	7.5	-	ns
t _{XSNR}	Exit self refresh to a Non-read command	t _{RFC} +10	-	t _{RFC} +10	-	ns
t _{XSRD}	Exit self refresh to a Read command	200	-	200	-	t _{CK}
t _{XP}	Exit precharge power down to any Non- read command	2	-	2	-	t _{CK}
t _{XARD}	Exit active power down to read command	2	-	2	-	t _{CK}
t _{XARDS}	Exit active power down to read command	7-AL	-	8-AL	-	t _{CK}
t _{CKE}	CKE minimum pulse width	3	-	3	-	t _{CK}
t _{AOND}	ODT turn-on delay	2	2	2	2	t _{CK}
t _{AON}	ODT turn-on	t _{AC} (min)	t _{AC} (max) +0.7	t _{AC} (min)	t _{AC} (max) +0.7	ns
t _{AONPD}	ODT turn-on (Power down mode)	t _{AC} (min) +2	2t _{CK} + t _{AC} (max) +1	t _{AC} (min) +2	2t _{CK} + t _{AC} (max) +1	ns
t _{AOFD}	ODT turn-off delay	2.5	2.5	2.5	2.5	t _{CK}
t _{AOF}	ODT turn-off	t _{AC} (min)	t _{AC} (max) +0.6	t _{AC} (min)	t _{AC} (max) +0.6	ns
t _{AOFPD}	ODT turn-off (Power down mode)	t _{AC} (min)+2	2.5t _{CK} + t _{AC} (max) +1	t _{AC} (min)+2	2.5t _{CK} + t _{AC} (max) +1	ns
t _{ANPD}	ODT to power down entry latency	3	-	3	-	t _{CK}
t _{XAPD}	ODT power down exit latency	8	-	8	-	t _{CK}

Speed Grade Definition

Symbol	Parameter	PC2-5300		PC2-6400		Unit
		Min	Max	Min	Max	
t _{RAS}	Row Active Time	45	70,000	45	70,000	ns
t _{RC}	Row Cycle Time	60	-	57.5	-	ns
t _{RCD}	RAS to CAS delay	15	-	12.5	-	ns
t _{RP}	Row Precharge Time	15	-	12.5	-	ns

Package Dimensions

(512MB, 1 Rank, 64Mx8 DDR2 SDRAMs)



Note: All dimensions are typical with tolerances of ± 0.15 (0.006) unless otherwise stated

Units: Millimeters (Inches)

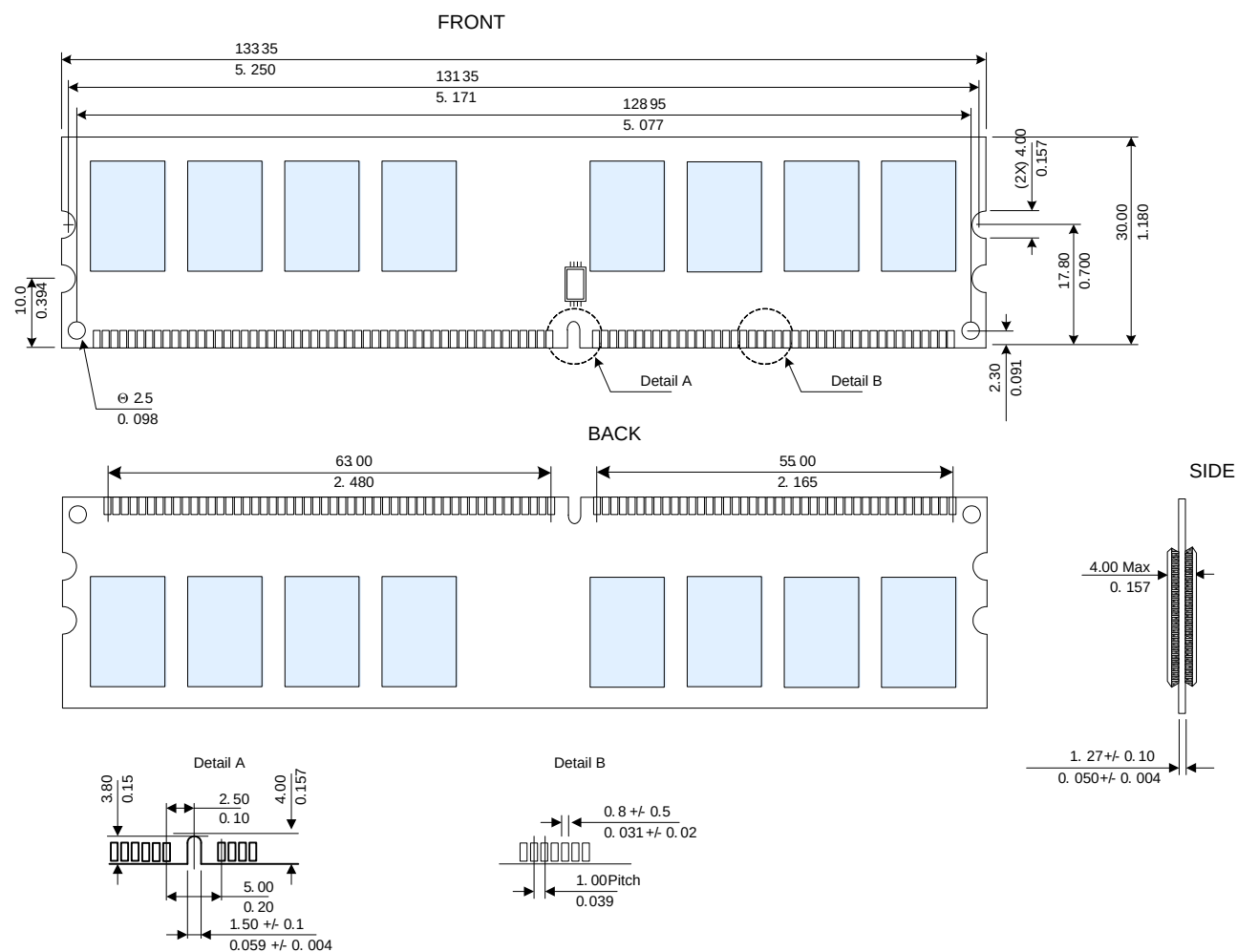
Note: Device position is only for reference.

REV 0.1

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Package Dimensions

(1GB, 2 Ranks, 64Mx8 DDR2 SDRAMs)

Note: All dimensions are typical with tolerances of ± 0.15 (0.006) unless otherwise stated

Units: Millimeters (Inches)

Note: Device position is only for reference.

REV 0.1

08/2008

Revision Log

Rev	Date	Modification
0.1	08/2008	Preliminary Release